

## CLAIMS

What is claimed is:

- 1        1.        A field effect transistor (FET) comprising:  
2                a fin formed on a dielectric surface;  
3                a device gate along one side of said fin;  
4                a back bias gate along an opposite side of said fin;  
5                device gate dielectric along one first side between said device gate and said fin;  
6        and  
7                back bias gate dielectric along said opposite side between said back bias gate and  
8        said fin; wherein said back bias gate dielectric differs from said device gate dielectric in  
9        at least one of material and thickness.
- 1        2.        A FET as in claim 1, wherein said fin is a semiconductor fin selected from a  
2        group of materials consisting of silicon, germanium and silicon-germanium.
- 1        3.        A FET as in claim 2, wherein said fin is a silicon fin.
- 1        4.        A FET as in claim 1, wherein one of said device gate dielectric and said back bias  
2        gate dielectric are a layered dielectric comprising at least 2 dielectric material layers.
- 1        5.        A FET as in claim 1, wherein said back bias gate dielectric is thicker than said  
2        gate dielectric.
- 1        6.        A FET as in claim 1, wherein each of said back bias gate dielectric and said gate  
2        dielectric is selected from a group of materials consisting of an oxide, an oxynitride and a  
3        high K dielectric.

YOR920030479US1

- 1 7. A FET as in claim 1, wherein said gate and said back bias gate are a conductive  
2 material selected from a group of materials consisting of a metal, doped silicon, doped  
3 germanium, doped silicon germanium and a metal silicide.
- 1 8. A FET as in claim 3, wherein said dielectric surface is an oxide layer.
- 1 9. A FET as in claim 8, wherein said oxide layer is a buried oxide layer.
- 1 10. A FET as in claim 8, wherein said oxide layer is disposed on a nitride layer.
- 1 11. A FET as in claim 3, further comprising a dielectric pillar above said silicon fin.
- 1 12. A FET as in claim 11, wherein said dielectric pillar is a nitride pillar.
- 1 13. A FET as in claim 12, wherein said nitride pillar forms a cap between said device  
2 gate and said back bias gate.
- 1 14. An integrated circuit (IC) on a semiconductor on insulator (SOI) chip, said IC  
2 including a plurality of field effect transistors (FETs) disposed on an insulating layer,  
3 each of said FETs comprising:  
4 a semiconductor fin formed on an insulating layer;  
5 device gate dielectric along a first side of said semiconductor fin;  
6 a device gate along said device gate dielectric;  
7 back bias gate dielectric along an opposite of said semiconductor fin;  
8 a back bias gate along said back bias gate dielectric; wherein said back bias gate  
9 dielectric differs from said device gate dielectric in at least one of material and thickness.
- 1 15. An IC as in claim 14, wherein said back bias gate dielectric is five times (5X)  
2 thicker than said gate dielectric.

YOR920030479US1

- 1        16.     An IC as in claim 14, wherein each of said back bias gate dielectric and said gate  
2        dielectric is selected from a group of materials consisting of an oxide, an oxynitride and a  
3        high K dielectric.
- 1        17.     An IC as in claim 14, wherein one of said device gate dielectric and said back bias  
2        gate dielectric are a layered dielectric comprising at least 2 dielectric material layers.
- 1        18.     An IC as in claim 14, wherein said gate and said back bias gate are a conductive  
2        material selected from a group of materials consisting of a metal, doped silicon, doped  
3        germanium, doped silicon germanium and a metal silicide.
- 1        19.     An IC as in claim 14, wherein said dielectric surface is an oxide layer.
- 1        20.     An IC as in claim 19, wherein said oxide layer is a buried oxide layer.
- 1        21.     An IC as in claim 19, wherein said oxide layer is disposed on a nitride layer.
- 1        22.     An IC as in claim 14, each said FET further comprising a dielectric pillar above  
2        said semiconductor fin.
- 1        23.     An IC as in claim 22, wherein said dielectric pillar is a nitride pillar.
- 1        24.     An IC as in claim 23, wherein said nitride pillar forms a cap between said device  
2        gate and said back bias gate.
- 1        25.     An IC as in claim 22, wherein said semiconductor is silicon.

1        26.     A method of forming an integrated circuit (IC), said method comprising the steps  
2        of:  
3                a)        forming semiconductor fins on a silicon on insulator (SOI) wafer;  
4                b)        forming back bias gates along one side of each of said semiconductor fins,  
5        said back bias gates comprising back bias gate dielectric; and  
6                c)        forming device gates along an opposite side of each of said semiconductor  
7        fins; said device gates comprising gate dielectric with at least one of material and  
8        thickness being different from said back bias gate dielectric.

1        27.     A method of forming an IC as in claim 26, wherein the semiconductor fin is a  
2        silicon fin and the step (a) of forming silicon fins comprises the steps of:  
3                i)        forming a pillar on a silicon layer;  
4                ii)       etching a portion of said silicon layer, a first side of said silicon fins being  
5        defined by removal of said portion;  
6                iii)       protecting said first side; and  
7                iv)       etching remaining portions of said silicon layer, a second side of said  
8        silicon fins being defined by removal of said portions, silicon fins  
9        remaining at said pillars a second.

1        28.     A method of forming an IC as in claim 27, wherein the semiconductor fin is a  
2        silicon fin and the step (i) of forming pillars comprises the steps of:  
3                A)        forming a dielectric layer on said silicon layer;  
4                B)        forming a sacrificial layer on said dielectric layer;  
5                C)        removing portions of said dielectric layer and said sacrificial layer; and  
6                D)        forming said pillars alongside remaining portions of said dielectric layer  
7        and said sacrificial layer.

1 29. A method of forming an IC as in claim 28, wherein forming pillars in step (D)  
2 comprises the steps of:

3 I) depositing a conformal layer on said SOI wafer; and

4 II) isotropically etching said conformal layer.

1 30. A method of forming an IC as in claim 29, wherein said conformal layer is a  
2 nitride layer.

1 31. A method of forming an IC as in claim 30, wherein said sacrificial layer is a layer  
2 comprising germanium (Ge).

1 32. A method of forming an IC as in claim 31, wherein said sacrificial layer is a  
2 polysilicon germanium (SiGe) layer.

1 33. A method of forming an IC as in claim 32, wherein the step (ii) of protecting the  
2 first side comprises depositing a second SiGe layer.

1 34. A method of forming an IC as in claim 27, wherein said silicon layer is on a  
2 layered dielectric and the step (iv) of etching remaining portions etches through upper  
3 layers of said layer dielectric to a buried oxide layer.

1 35. A method of forming an IC as in claim 34, wherein said upper layers comprise an  
2 oxide layer on a nitride layer and said nitride layer is on said buried oxide layer.

1 36. A method of forming an IC as in claim 27, wherein the step (b) of forming back  
2 bias gates comprises:

3 i) forming a back bias gate dielectric layer;

4 ii) forming a back bias gate layer on said back bias gate dielectric layer;

5 iii) depositing a fill material;

6           iv)     planarizing an upper surface of said SOI wafer; and  
7           v)     removing portions of said back bias gate layer and said back bias gate  
8           dielectric layer such that each of said pillars are exposed.

1       37.     A method of forming an IC as in claim 36, wherein planarizing the upper surface  
2       in step (b)(iv) comprises depositing fill material and polishing with a chemical  
3       mechanical polish (CMP) to planarized said wafer.

1       38.     A method of forming an IC as in claim 37, wherein removing portions in step  
2       (b)(v) comprises continuing CMP and stopping on said pillar.

1       39.     A method of forming an IC as in claim 37, wherein the step (b) of forming back  
2       bias gates further comprises:

3           vi)     forming voids between said pillars and remaining said portions of said  
4       back bias gate layer;  
5           vii)    filling said voids.

1       40.     A method of forming an IC as in claim 36, wherein the step (c) of forming device  
2       gates comprises:

3           i)     re-exposing said first side;  
4           ii)    forming a gate dielectric layer;  
5           iii)   forming a gate layer on said wafer;  
6           iv)    removing portions of said gate layer, device gates being separated from  
7       back bias gates and each of said pillars being exposed.

1       41.     A method of forming an IC as in claim 40, wherein said gate dielectric layer is  
2       one fifth as thick as said back bias dielectric layer.

1 42. A method of forming an IC as in claim 41, wherein said gate dielectric layer is  
2 selected from a group of materials consisting of an oxide, an oxynitride and a high K  
3 dielectric.

1 43. A method of forming an IC as in claim 40, wherein said gate layer is the same  
2 material as said back bias gate layer.

1 44. A method of forming an IC as in claim 43, wherein said gate layer and said back  
2 bias gate layer are polysilicon layers.

1 45. A method of forming an IC as in claim 44, wherein the step (c)(ii) of forming the  
2 gate layer comprises the steps of:

- 3 A) forming polysilicon spacers on both sides of said fins, said polysilicon  
4 spacers being separated from said fins on said opposite side by said gate dielectric layer;  
5 B) removing horizontal portions of said gate dielectric layer; and  
6 C) depositing a polysilicon layer.

1 46. A method of forming an IC as in claim 45, wherein the step (c)(iv) of removing  
2 portions of the gate layer comprises the steps of:

- 3 A) directionally depositing a dielectric layer; and  
4 B) selectively removing horizontal portions of the directionally deposited said  
5 dielectric layer, portions of said polysilicon gate layer above said pillars being exposed;  
6 and  
7 C) isotropically etching said polysilicon gate layer.

1        47.    A method of forming an IC as in claim 46, wherein the step (c)(iv) of forming  
2        back bias gates further comprises:  
3                D)    forming voids between said pillars and remaining said portions of said  
4        gate layer;  
5                E)    filling said voids.